

Ambient Light Sensor IC Series

Digital 16bit Serial Output Type Ambient Light Sensor IC



BH1780GLI No.09046EAT08

Descriptions

BH1780GLI is an digital Ambient Light Sensor IC for I^2C bus interface. This IC is the most suitable to obtain the ambient light data for adjusting LCD and Keypad backlight power of Mobile phone. It is possible to detect wide range at High resolution. (1 - 65535 lx).

Features

- 1) I²C bus Interface (F/S mode & Hs mode Support, Slave address: "0101001")
- 2) Spectral responsibility is approximately human eye response
- 3) Illuminance to Digital Converter
- 4) Wide range and High resolution. (1-65535 lx)
- 5) Low Current by power down function
- 6) 50Hz / 60Hz Light noise reject-function
- 7) 1.8V Logic input interface
- 8) No need any external parts
- 9) Light source dependency is little. (ex. Incandescent Lamp. Fluorescent Lamp. Halogen Lamp. White LED. Sun Light)
- 10) Small measurement variation (+/- 20%)
- 11) The influence of infrared is very small.

Applications

Mobile phone, LCD TV, NOTE PC, Portable game machine, Digital camera, Digital video camera, Car navigation, PDA, LCD display

Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	Vmax	4.5	V
Operating Temperature	Topr	-40~85	°C
Storage Temperature	Tstg	-40~100	°C
SDA Sink Current	Imax	7	mA
Power Dissipation	Pd	120※	mW

^{※ 70}mm × 70mm × 1.6mm glass epoxy board. Derating in done at 1.6mW/°C for operating above Ta=25°C.

Operating Conditions

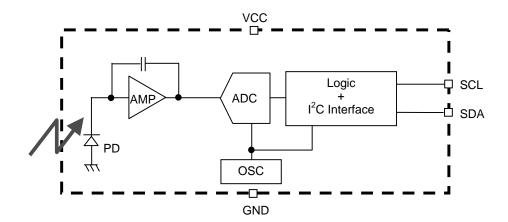
Parameter	Symbol	Min.	Тур.	Max.	Units
VCC Voltage	Vcc	2.3	2.5	3.0	٧

● Electrical Characteristics (VCC = 2.5V, Ta = 25°C, unless otherwise noted)

Powerdown Current Measurement Accuracy Dark (0 lx) Sensor out Measurement Time SCL SDA input 'H' Voltage SCL SDA input 'H' Voltage SCL SDA input 'H' / 'L' Current I^2C SDA Output 'L' Voltage V I^2C Rejected Spike pulse witdh I^2C Rejected Spike pulse witdh I^2C Rejected Spike pulse witdh2 SDA SCL Capacitance I^2C SCL Clock Frequency I^2C SCL Clock Frequency I^2C Hold Time (Repeated) START Condition I^2C Hold Time (Repeated) START Condition2 I^2C 'L' Period of the SCL Clock I_2C 'L' Period of the SCL Clock2	cc1 cc2 cc2 cc2 cc2 cc2 cc2 cc2 cc2 cc2	- - 0.8	120 0.7	200 2.5	uA	Ev=100 lx ※
Measurement Accuracy Dark (0 Ix) Sensor out Measurement Time SCL SDA input 'H' Voltage SCL SDA input 'H' Voltage SCL SDA input 'H' / 'L' Current I^2C SDA Output 'L' Voltage V I^2C Rejected Spike pulse witdh I^2C Rejected Spike pulse witdh I^2C Rejected Spike pulse witdh2 SDA SCL Capacitance I^2C SCL Clock Frequency I^2C SCL Clock Frequency I^2C Hold Time (Repeated) START Condition I^2C Hold Time (Repeated) START Condition2 I^2C 'L' Period of the SCL Clock I_2C 'L' Period of the SCL Clock2	5/A 50	0.8		2.5		
Dark (0 lx) Sensor out Measurement Time SCL SDA input 'H' Voltage SCL SDA input 'L' Voltage SCL SDA input 'H' / 'L' Current I^2C SDA Output 'L' Voltage V I^2C Rejected Spike pulse witdh t I^2C Rejected Spike pulse witdh t SDA SCL Capacitance I^2C SCL Clock Frequency I^2C SCL Clock Frequency I^2C Hold Time (Repeated) START Condition I^2C Hold Time (Repeated) START Condition2 I^2C 'L' Period of the SCL Clock I_2C 'L' Period of the SCL Clock2 I_2C 'L' Period of the SCL Clock2	50		4.0		uA	No Input Light
Measurement Time SCL SDA input 'H' Voltage SCL SDA input 'L' Voltage SCL SDA input 'H' / 'L' Current I²C SDA Output 'L' Voltage V I²C Rejected Spike pulse witdh t²C Rejected Spike pulse witdh2 SDA SCL Capacitance I²C SCL Clock Frequency fs I²C SCL Clock Frequency2 fs I²C Hold Time (Repeated) START Condition I²C Hold Time (Repeated) START Condition2 I²C 'L' Period of the SCL Clock tL I²C 'L' Period of the SCL Clock2		0	1.0	1.2	Times	Sensor out / Actual lx Ev=1000 lx ※
SCL SDA input 'H' Voltage SCL SDA input 'L' Voltage SCL SDA input 'H' / 'L' Current I^2C SDA Output 'L' Voltage V I^2C Rejected Spike pulse witdh I^2C Rejected Spike pulse witdh2 SDA SCL Capacitance I^2C SCL Clock Frequency I^2C SCL Clock Frequency I^2C Hold Time (Repeated) START Condition I^2C Hold Time (Repeated) START Condition2 I^2C 'L' Period of the SCL Clock I_2C 'L' Period of the SCL Clock2 I_2C 'L' Period of the SCL Clock2	N /	0	0	2	count	
SCL SDA input 'L' Voltage SCL SDA input 'H' / 'L' Current I²C SDA Output 'L' Voltage V I²C Rejected Spike pulse witdh t I²C Rejected Spike pulse witdh2 SDA SCL Capacitance I²C SCL Clock Frequency fs I²C SCL Clock Frequency2 fs I²C Hold Time (Repeated) START Condition I²C Hold Time (Repeated) START Condition2 I²C 'L' Period of the SCL Clock t I²C 'L' Period of the SCL Clock2	M	_	150	250	ms	
SCL SDA input 'H' / 'L' Current I^2C SDA Output 'L' Voltage V I^2C Rejected Spike pulse witdh I^2C Rejected Spike pulse witdh2 SDA SCL Capacitance I^2C SCL Clock Frequency I^2C SCL Clock Frequency2 I^2C Hold Time (Repeated) START Condition I^2C Hold Time (Repeated) START Condition2 I^2C 'L' Period of the SCL Clock I^2C 'L' Period of the SCL Clock2	/ _{ІН}	1.26	_	_	V	
I ² C SDA Output 'L' Voltage V I ² C Rejected Spike pulse witdh I ² C Rejected Spike pulse witdh2 SDA SCL Capacitance I ² C SCL Clock Frequency I ² C SCL Clock Frequency fs I ² C Hold Time (Repeated) START Condition I ² C Hold Time (Repeated) START Condition2 I ² C 'L' Period of the SCL Clock I ² C 'L' Period of the SCL Clock2	/ _{IL}	_	-	0.54	V	
I ² C Rejected Spike pulse witdh I ² C Rejected Spike pulse witdh2 SDA SCL Capacitance I ² C SCL Clock Frequency I ² C SCL Clock Frequency2 I ² C Hold Time (Repeated) START Condition I ² C Hold Time (Repeated) START Condition2 I ² C 'L' Period of the SCL Clock I ² C 'L' Period of the SCL Clock2	I _i	-10	_	10	uA	
I ² C Rejected Spike pulse witdh2 SDA SCL Capacitance I ² C SCL Clock Frequency I ² C SCL Clock Frequency2 I ² C Hold Time (Repeated) START Condition I ² C Hold Time (Repeated) START Condition2 I ² C 'L' Period of the SCL Clock I ² C 'L' Period of the SCL Clock2	OL1	0	_	0.4	V	IOL=3 mA
SDA SCL Capacitance I²C SCL Clock Frequency I²C SCL Clock Frequency2 I²C Hold Time (Repeated) START Condition I²C Hold Time (Repeated) START Condition2 I²C 'L' Period of the SCL Clock I²C 'L' Period of the SCL Clock2	SP	-	100	-	ns	F/S mode
I ² C SCL Clock Frequency I ² C SCL Clock Frequency2 I ² C Hold Time (Repeated) START Condition I ² C Hold Time (Repeated) START Condition2 I ² C 'L' Period of the SCL Clock I ² C 'L' Period of the SCL Clock2 I ² C 'L' Period of the SCL Clock2	SP	-	20	-	ns	Hs mode
I ² C SCL Clock Frequency2 I ² C Hold Time (Repeated) START Condition I ² C Hold Time (Repeated) START Condition2 I ² C 'L' Period of the SCL Clock I ² C 'L' Period of the SCL Clock2 I ² C 'L' Period of the SCL Clock2	Ci	-	7	-	pF	
I²C Hold Time (Repeated) START Condition tHE I²C Hold Time (Repeated) START Condition2 tHE I²C 'L' Period of the SCL Clock tL I²C 'L' Period of the SCL Clock2 tL	SCL	_	_	400	kHz	F/S mode
Condition I ² C Hold Time (Repeated) START Condition2 I ² C 'L' Period of the SCL Clock I ² C 'L' Period of the SCL Clock2 t _L	CLH	0	-	3.4	MHz	Hs mode Cb=100pF
$ \begin{array}{c} \text{I}^2\text{C Hold Time (Repeated) START} \\ \text{Condition2} \\ \text{I}^2\text{C 'L' Period of the SCL Clock} \\ \text{I}^2\text{C 'L' Period of the SCL Clock2} \\ \end{array} $	D;STA	0.6	_	_	us	F/S mode
I ² C 'L' Period of the SCL Clock2 t _L);STA	160	-	-	ns	Hs mode
2	OW	1.3	_	_	us	F/S mode
J ² C 'H' Period of the SCL Clock tu	OW	160	-	_	ns	Hs mode
I O II I CIIOG OI IIIC OOL OIOOK	IIGH	0.6	_	_	us	F/S mode
I ² C 'H' Period of the SCL Clock2	IGH	60	-	_	ns	Hs mode
I ² C Set up time for a Repeated START Condition	J;STA	0.6	_	_	us	F/S mode
I ² C Set up time for a Repeated START Condition2	J;STA	160	_	_	ns	Hs mode
I ² C Data Hold Time t _{HE});DAT	0	_	_	us	F/S mode
I ² C Data Hold Time2 t _{HC});DAT	0	_	70	ns	Hs mode Cb=100pF
I ² C Data Setup Time t _{SU}	J;DAT	100	_	_	ns	F/S mode
I ² C Data Setup Time2 t _{SL}	J;DAT	10	_	_	ns	Hs mode
I ² C Set up Time for STOP Condition	I;STO	0.6	_	_	us	F/S mode
I ² C Set up Time for STOP Condition2	I;STO	160	_	_	ns	Hs mode
I ² C Bus Free Time between a STOP and START Condition	BUF	1.3	_	_	us	
I ² C Data Valid Time t _{VE});DAT	-	-	0.9	us	F/S mode
I ² C Data Valid Acknowledge Time t _{VE}		_	-	0.9	us	F/S mode

White LED is used as optical source.

Block Diagram



- PD
 - Photo diode with approximately human eye response.
- AMP
 - Integration-OPAMP for converting from PD current to voltage.
- ADC
 - AD converter for obtainment digital 16bit data.
- Logic + I²C Interface
 - Ambient Light Calculation and I²C bus Interface. It is including below register.
 - Data Register → This is for registration of Ambient Light Data. Initial Value is "0000_0000_0000_0000".
- OSC
 - Internal Oscillator (typ. 320kHz). It is CLK for internal logic.

Technical Note

Reference Data

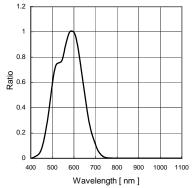


Fig.1 Spectral Response

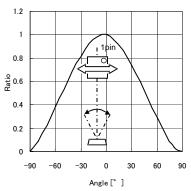


Fig.4 Directional Characteristics 1

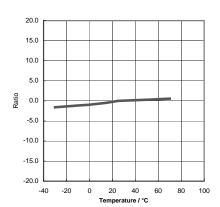


Fig.7 Measurement Result Temperature Dependency

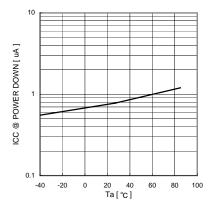
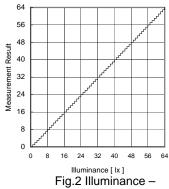


Fig.10 VCC - ICC@0 Lx (POWER DOWN)



Measurement Result 1

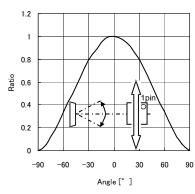


Fig.5 Directional Characteristics 2

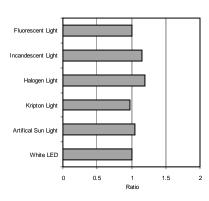


Fig.8 Light Source Dependency (Fluorescent Light is set to '1')

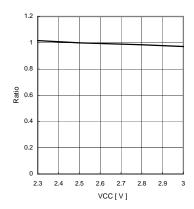


Fig.11 Measurement Result VCC Dependency

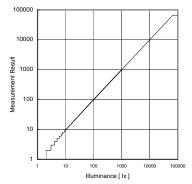


Fig.3 Illuminance -Measuremnet Result 2

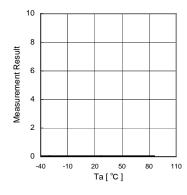


Fig.6 Dark Response

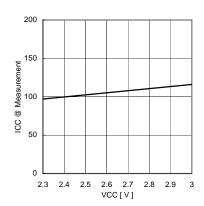


Fig.9 VCC - ICC (During measurement)

Command Set

Address	Register name	Register function
	COMMAND	Specifies register address
0h	CONTROL	Control of basic functions
Ah	PART ID	Part ID
Bh	MANUFACTURE ID	Manufacture ID
Ch	DATALOW	Low byte of ADC
Dh	DATAHIGH	High byte of ADC

O Command Register

7	6	5	4	3	2	1	0
CMD	XXX				ADDF	RESS	

default value 00h

Field	Bit	Description
CMD	7	Write 1
xxx	6:4	Write "000" Don't care if ADDRESS(Command Register< 3 : 0 >) is "0h" or "Ah" or "Bh" or "Ch" or "Dh".
ADDRESS	3:0	Register address

O Control Register (0h)

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	RES	POV	VER

default value 00h

Field	Bit	Description	
RES	7:2	Write "000000"	
POWER	1:0	"00" : Power down "01" : Resv "10" : Resv "11" : Power up	

O PART ID Register (Ah)

The PART ID register provides device identification. It is a read only register.

7	6	5	4	3	2	1	0
PART NO					RI	- v	

Field	Bit	Description
PARTNO	7 : 4	"1000"
REV	3:0	"0001"

O MANUFATCURE ID Register (Bh)

The MANUFACTURE ID register provides device identification. It is a read only register.

7	6	5	4	3	2	1	0	
MANUFACTURE ID								

Field	Bit	Description
MANUFACTURE ID	7:0	"0000001"

O ADC channel data registers (Ch, Dh)

Illuminance data register.

7	6	5	4	3	2	1	0
			CHANN	NEL DATA			

Register	Address	Bit	Description
DATALOW	Ch	7:0	Lower byte
DATAHIGH	Dh	7:0	Upper byte

Lux calculation

Measurement result is registered to ADC channel data registers(Ch, Dh) in below format.

DATALOW (Ch)

7	6	5	4	3	2	1	0
2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 °

DATAHIGH (Dh)

I	7	6	5	4	3	2	1	0
	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	211	2 ¹⁰	2 ⁹	2 ⁸

This is an example for DATA to Lux convertion when DATA Register values are seeing in below condition. ex)

DATA Low Byte = "1001_0000" DATA High Byte = "1000_0011"

$$(2^{15} + 2^9 + 2^8 + 2^7 + 2^4) = 33680 [Ix]$$

			from Slave to Mastel	_	
	from Master to Slave		Irom Slave to Master		
① Send Pov	wer up instruction.				
ST	Slave Address 0101001	W ACK	Command Register 10000000	AC	CK
	Co	ontrol Register (0h) 00000011	ACK SP		
② Change A	ADDRESS Field of Control Re			_	
ST	Slave Address 0101001	W ACK	Command Register 10001100	ACK	
③ Read me	until Measurement result is ou	nput.			
③ Read mea		R ACK	DATALOW (Ch)	ļ	40
	asurement result. Slave Address 0101001	R ACK	DATALOW (Ch)	A	40
ST	asurement result. Slave Address 0101001	R 1 ACK DATAHIGH (Dh)		<i>A</i>	40
ST S	asurement result. Slave Address 0101001	R 1 ACK DATAHIGH (Dh)			40
ST S	asurement result. Slave Address 0101001 ms until measurement result is	R 1 ACK DATAHIGH (Dh)			
Wait 150r Read mea	asurement result. Slave Address 0101001 ms until measurement result is asurement result. Slave Address 0101001	R ACK DATAHIGH (Dh) s updated.	ACK SP		
Wait 150r Read mea	asurement result. Slave Address 0101001 ms until measurement result is asurement result. Slave Address 0101001	R ACK DATAHIGH (Dh) s updated.	DATALOW (Ch)		
Wait 150r Read mea	asurement result. Slave Address 0101001 ms until measurement result is asurement result. Slave Address 0101001	R ACK DATAHIGH (Dh) s updated.	DATALOW (Ch)		4400

- I²C Bus Communication
 - 1) Slave Address "0101001"
 - 2) Main write Format
 - 1. Write to Command Register

ST	Slave Address 0101001	W 0	ACK	Data to Command Register 1000XXXX	ACK	SP	
----	--------------------------	--------	-----	--------------------------------------	-----	----	--

X Data<7:4> must be "1000"

2. Write to Control Register

ST	Slave Address 0101001	W 0	ACK	Data to Control Register 000000XX	ACK	SP	
----	--------------------------	--------	-----	--------------------------------------	-----	----	--

X Data<7:2> must be "000000"

X It is necessary that ADDRESS Field of Command Register must set "0000".

3. Write to Command Register and Control Register

ST	Slave Address 0101001	W 0	ACK	Command Register 1000XXXX	ACK]
----	--------------------------	--------	-----	------------------------------	-----	---

Control Register (0h) 000000XX	ACK	SP
-------------------------------------	-----	----

3) Main read Format

ST Slave Address R 1 ACK Data specified at ADDRESS Field of Command Register
--

Data specified at ADDRESS Field of Command Register+1	ACK		ACK	Data specified at ADDRESS Field of Command Register +N	IACK	SP
---	-----	--	-----	---	------	----

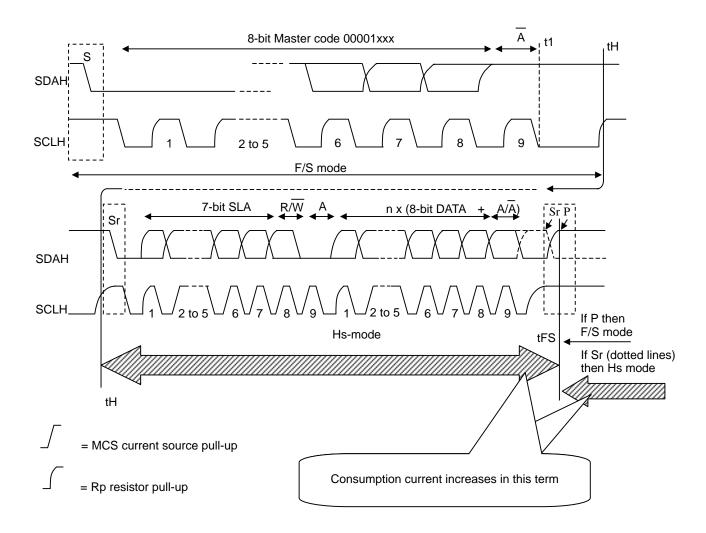
0h - Ah - BH1780GLI outputs Data from specified ADDRESS Field of Command Register until Master issues stop condition.Read cycle is Bh - Ch - Dh - 0h - Ah - Bh - Ch - Dh

ex) If ADDRESS Field of Command Register is Ch, then BH1780GLI outputs data like seeing in below. Ch - Dh - Oh - Ah - Bh - Ch - Dh - Oh - Ah It is continued until Master issues stop condition.

4) High speed mode

BH1780GLI supports I^2C bus High speed mode (Hs-mode). Approximately 80uA is consumped when I^2C bus is set at Hs-mode. Typical consumption current is seeing in below table.

State	F/S mode	Hs-mode	unit
Power down	0.7	80	uA
Power up	120	200	uA



Caution of power on reset function

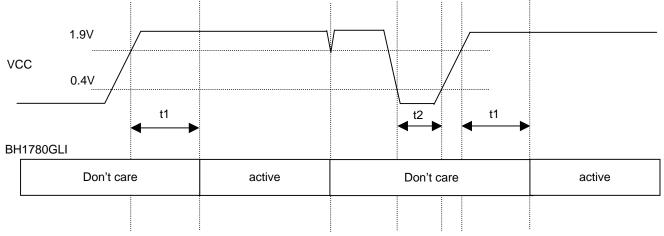
BH1780GLI has power on reset (POR) function. POR is to reset all register and flip flop when VCC Power supplies. There is some cautions about power on and down sequence seeing in below.

1 Power on time: t1

More than 2ms is need to active BH1780GLI after VCC supplies more than 1.9V from VCC is less than 0.4V.

2 Power off time : t2

More than 1ms (VCC < 0.4V) is need to active BH1780GLI.

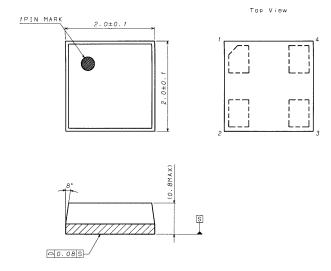


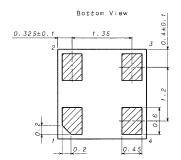
^{*&}quot;active state" is that BH1780GLI works and accept I²C bus access correctly.

Terminal Description

PIN No.	Terminal Name	Equivalent Circuit	Function
1	VCC		Power Supply Terminal
2	GND		GND Terminal
3	SDA		I ² C bus Interface SDA Terminal
4	SCL		I ² C bus Interface SCL Terminal

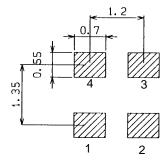
Package Outlines





(UNIT:mm)

Recommended Land pattern (Top view)



Cautions on use

1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage (Vmax), temperature range of operating conditions (Topr), etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

2) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

3) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

4) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

5) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals; such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate.

7) Thermal design

Perform thermal design in which there are adequate margins by taking into account the power dissipation (Pd) in actual states of use.

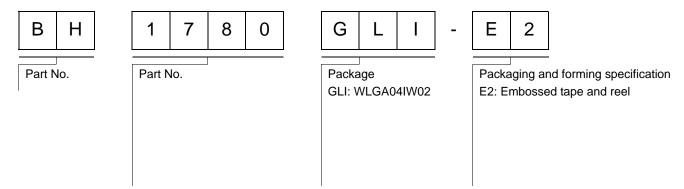
8) Treatment of package

Dusts or scratch on the photo detector may affect the optical characteristics. Please handle it with care.

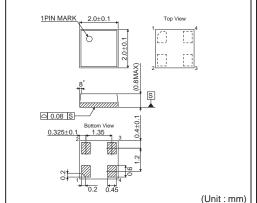
9) Rush current

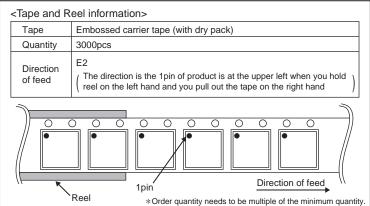
When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

Ordering part number



WLGA04IW02





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